REMARKS

Claims 1-19 are presented for examination.

Claims 1-4, 6, 7 and 9-19 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Sainton et al. in view of Norman. Dependent claims 5, 6, 16 and 18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Sainton et al. and Norman, in view of Bowen et al.

These rejections are respectfully traversed for the following reasons.

In the application of a rejection under 35 U.S.C. §103, it is incumbent upon the Examiner to factually support a conclusion of obviousness. As stated in ***Graham v. John Deere Co.*** 383 U.S. 1, 13, 148 U.S.P.Q. 459, 465 (1966), obviousness under 35 U.S.C. §103 must be determined by considering (1) the scope and content of the prior art; (2) ascertaining the differences between the prior art and the claims in issue; and (3) resolving the level of ordinary skill in the pertinent art.

However, as demonstrated below, the Examiner has failed to ascertain the differences between the prior art and the claims in issue. In particular, claim 1 recites a memory system for a portable telephone including a signal transmission/reception portion for transmitting and receiving a signal and a control portion for controlling at least a signal transmission and reception operation of said transmission/reception portion.

The memory system comprises:

- a random access memory providing a working area for said control portion; and

- a flash memory including a memory array for storing a program for said control portion and at least transmission and reception data in a non-volatile manner under a control of said control portion.

Claim 1 specifies that the memory array is divided into a plurality of storage units, and a register, provided commonly to the respective storage units, and having information in a storage unit of said plurality of storage units transmitted thereinto for temporal storage of the transmitted information and allowing serial readout of the transmitted and stored information.

Further, independent claim 12 also recites that the memory array is divided into a plurality of storage units. The claim specifies that a plurality of pieces of information in one unit of the storage units selected in accordance with an address signal at a time, are allowed to be serially read out in synchronization with a clock signal without further address application.

The Examiner takes the position that Sainton discloses a memory providing a working area for said control portion; and a memory for storing a program for said control portion and at least transmission and reception data in a non-volatile manner under a control of said control portion.

However, the Examiner has failed to point out specifically which memories of Sainton correspond to the claimed memories.

Further, the Examiner admits that Sainton has failed to disclose the claimed flash memory having a divided memory array. She relies upon Norman for disclosing the claimed arrangement.

However, the Examiner has failed to point out specifically which elements of Norman are considered to correspond to the claimed elements. Instead, she relied upon col. 2, line 12 to col. 4, line 38, and col. 5, line 57 to col. 6, line 65 for disclosing the flash memory arrangement recited in claim 1.

Moreover, the Examiner has failed to address the memory array arrangement recited in claim 12.

Accordingly, the Examiner has failed to ascertain the differences between the prior art and the claims in issue.

Considering the references, Sainton discloses an omni-modal communication device for accommodating a plurality of communication systems. In Sainton, necessary information for each communication mode (system) is stored in memory 112, and the communication pursuant to a selected communication mode is enabled in accordance with the program and control information stored in memory 112.

As discussed above, the Examiner. did not indicate which memory of Sainton corresponds to the claimed flash memory. However, it appears that memory 112 shown in Fig. 1B is considered to correspond to the claimed flash memory in view of the disclosure referred to by the Examiner in the Office action. Memory 112 stores the information and program required for the microprocessor 110 to perform a process such as the protocol of data transmission and reception.

However, memory 112 of Sainton is not used for storing the transmission and reception data. Transmission and reception data transferred via data input 114 and data output 116 are processed by data processing circuit 118, and the connecting destination of data processing circuit 118 is determined and established by the microprocessor in accordance with the program stored in memory 112.

By contrast, the claims 1 and 12 specifically require the claimed flash memory to store a program for the control portion and at least transmission and reception data in a non-volatile manner. Hence, memory 112 of Sainton does not correspond to the claimed flash memory.

In Sainton, the transmission and reception data are stored in memory 308 in Fig. 3. However, this memory is contained in a personal computer which performs communication

through the omni-modal circuit. Therefore. the memory 308 in the personal computer is not used for storing a program for the control portion. Accordingly, the memory 308 also cannot correspond to the claimed flash memory for storing a program for the control portion and at least transmission and reception data in a non-volatile manner.

Hence, Sainton does not disclose any memory arrangement for storing a program for the control portion and at least transmission and reception data in a non-volatile manner.

Norman discloses a flash management defect management system that includes a memory array having multiple memory cells 104. A shift register placed outside the flash memory identifies data at a failure address and writes these data into the overhead portion in the memory array, and also writes a dedicated bit to the failure address. Data are written in units of sectors and transferred in units of bytes to be stored in the input register (input latch) of the flash memory.

During data reading of Norman, the data stored in the overhead portion are externally read in parallel into the shift register for storage, and the data are read out in units of bytes from the flash memory, and the read out data at the failure address is replaced with the data in the shift register and then the read out data are stored in the buffer memory. Therefore, the data reading is performed without using the input register (input latch) and the data read out after replacement processing are sequentially stored in the buffer memory, and then the data arc sequentially read out from the buffer memory.

Hence, the input latch of Norman does not correspond to the claimed register, provided commonly to the respective storage units, and having information in a storage unit of said plurality of storage units transmitted thereinto for temporal storage of the transmitted information and allowing serial readout of the transmitted and stored information, as claim 1 requires.

Further, claim 12 recites that a plurality of pieces of information in one unit of the storage units selected in accordance with an address signal at a time, are allowed to be serially read out in synchronization with a clock signal without further address application.

By contrast, Norman discloses that data are read out and transferred in units of bytes to be stored in the buffer memory. For each read data, an address is generated for identifying the failure address and it is reasonable to use the address for designating the memory location for each byte data. Therefore, the data in a sector of Norman are not read out in parallel in response to one time application of an address signal.

Hence, Norman does not disclose the arrangement recited in claim 12.

It is well settled that the test for obviousness is what the combined teachings of the references would have suggested to those having ordinary skill in the art. ***Cable Electric Products, Inc. v. Genmark, Inc.***, 770 F.2d 1015, 226 USPQ 881 (Fed. Cir. 1985). In determining whether a case of *prima facie* obviousness exists, it is necessary to ascertain whether the prior art teachings appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification. ***In re Lalu***, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1984).

However, as demonstrated above, neither Sainton nor Norton discloses a flash memory (or any other memory unit) including a memory array for storing a program for the control portion and at least transmission and reception data in a non-volatile manner under a control of the control portion, as the claims require.

Further, neither Sainton nor Norton discloses the arrangements of the memory array specified in claims 1 and 12.

Accordingly, combined teachings of these references are not sufficient to arrive at the inventions recited in claims 1 and 12.

Moreover, in rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to provide a reason why one having ordinary skill in the art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or inference in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. ***Uniroyal, Inc. v. Rudkin-Wiley***, 837 F.2d 1044, 5 USPQ 2d 1434 (Fed. Cir. 1988); ***Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.***, 776 F.d 281, 227 USPQ 657 (Fed. Cir. 1985); ***ACS Hospital Systems, Inc. v. Montefiore Hospital***, 732 F.2d 1572, 221 USPQ 929 (Fed. Cir. 1984); ***In re Sernaker***, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983).

These showings by the Examiner are an essential part of complying with the burden of presenting a *prima facie* case of obviousness. ***In re Oetiker***, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

As demonstrated below, the Examiner has failed to provide proper reasons for combining the references and thus to establish a *prima facie* case of obviousness.

In particular, the Examiner has taken the position that it would have been obvious "to modify Sainton to include a random memory access memory and a flash memory for the purpose transferring serially, data bits from one memory cells to another."

However, the Examiner offered no logical reason, and no such reason is apparent, to support the conclusion that one having ordinary skill in the art would have been impelled to modify Sainton to include the claimed random memory access memory and flash memory. It is not apparent why one skilled in the art would have recognized any advantage to be gained by the proposed combination of references.

It is noted that Sainton discloses a radio processing circuit having memory 112. As the Examiner admits, Sainton does not have a flash memory. Moreover, one skilled in the art would realize that Sainton does not need a flash memory structure having a divided memory array and a register, provided commonly to the respective storage units, and allowing serial readout of the transmitted and stored information.

Also, one skilled in the art would realize that Sainton does not need "a random memory access memory and a flash memory for the purpose transferring serially, data bits from one memory cells to another." The prior art provides no reason for such a modification.

Accordingly, the Examiner's reasons for combining the references are improper.

Hence, Applicants submit that the combination of references applied by the Examiner does not teach or suggest the claimed invention. Therefore, the Examiner has failed to establish a case of *prima facie* obviousness. Moreover, the lack of any motivation for the proposed combination of references to arrive at the claimed invention further undermines the basis for the Examiner's rejection under 35 U.S.C. § 103.

Applicants, therefore, respectfully submit that the rejections of the claims under 35 U.S.C. § 103 are improper and should be withdrawn.

In view of the foregoing, and in summary, claims 1-19 are considered to be in condition for allowance. Favorable reconsideration of this application is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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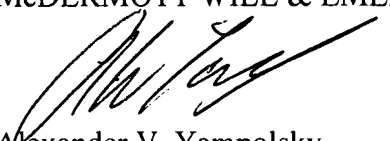

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